



## 7-Days Self-Sponsored Hybrid mode Workshop

On

# Chip Design Flow: Behavioral to Layout

May 16-22, 2024

### About the Institute

ABV-IIITM Gwalior is a premier institute incepted by MHRD, Government of India, in the year 1997 as a center of excellence in the field of Information Technology and Management. It is NAAC 'A' certified and has also been declared as an institute of national importance by the Government of India. It is located in the city of Gwalior in the northern part of the state of Madhya Pradesh, India. For more information, please visit: <http://iiitm.ac.in/>

### Who can Attend?

This is a programme designed for students, research scholars, professionals, faculty members, and others. The applicants are also welcome but not limited to B.Sc./M.Sc., B.E./B.Tech., M.E./M.Tech., Ph.D., working professionals from start-ups, MSMEs, and others.

### Topics to be covered

Mode of the course: Online/Offline

	<b>Session 1</b> 11:00 AM – 12:30 PM	<b>Session 2</b> 2:00 PM- 5:30 PM (Hands-on)
Day 1	Inauguration & Expert talk	Behavior coding Guidelines and Reference Digital Design
Day 2	Expert talk	Basics of Synthesis, DFT Insertion
Day 3	Expert talk	Basics of Physical Design Flow, Floor Plan, Power plan
Day 4	Expert talk	Basics of CTS, Routing, Timing, layout Verification-I
Day 5	Expert talk	Basics of CTS, Routing, Timing, layout Verification-II
Day 6	Expert talk	Case Study-1: Traffic Light Controller
Day 7	Expert talk	Case Study-2: Synchronous FIFO and Valedictory

- Study materials and Certificate will be provided to all the participants.
- The student will be technically benefited for internship and job placement in VLSI Companies like Synopsys, Cadence, HT Microelectronics, Micron, Qualcomm, etc./Projects/Higher studies.

### Resource Persons

Faculty members from IITs, IIITs and NITs and Industry experts shall deliver lectures and hands-on.

### Objectives

- Enhance the knowledge and skills of the participants in various steps of VLSI Physical Design like Partitioning, Chip planning, Placement, Routing and STA etc.
- Provides a hands-on training to get real-time knowledge about RTL to IC design with incorporate the Macro IP .
- Familiarize every participant with the latest trends and advancements of Chip Design Flow.

### Registration Fee

Student (online/Offline)	: INR (1000/1200)/-
Faculty Members (Online/Offline)	: INR (1400/1600)/-
Faculty Early Bird registration before or on 30 April 2024 (Online/Offline)	: INR (1200/1400)/-
Industry	: INR 2000/-

The lodging and food facility may be provided in the hostel/guest house as per the institute norms by their own expense.

Account Name : Director, ABV-IIITM, Gwalior  
Account Number : 945210110009380  
Bank name : Bank of India  
& IFSC Code : BKID0009462  
Branch Address : IIITM Branch Gwalior

Chief Patron: Prof. Sri Niwas Singh  
Director, ABV-IIITM Gwalior  
Patron: Prof. Manisha Pattanaik  
H.O.D., Electrical and Electronics Engineering  
Course Coordinators:  
Dr. Gaurav Kaushal, Dr. Somesh Kumar  
Course co-coordinators:  
Dr. Alok Kumar kamal, Dr. Biswabandu Jana

### Registration Link:

<https://forms.gle/jHgexJcHW1qGB2yA6>

Scan here for registration



Contact Us: Email: [kaushalg@iiitm.ac.in](mailto:kaushalg@iiitm.ac.in)  
Mob. No. : +91 7070895548

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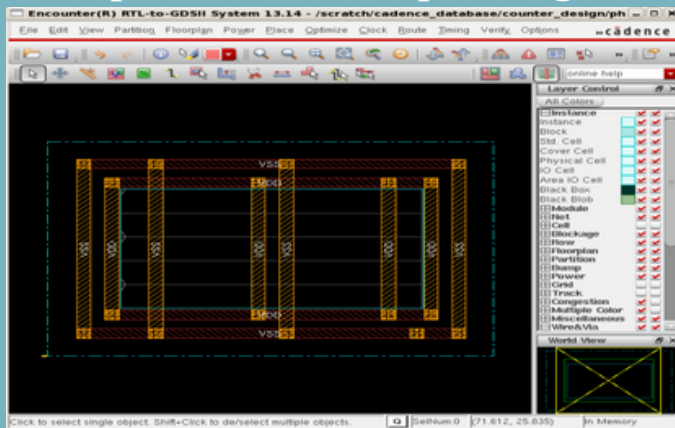
### About the Programme

The workshop is a 7-day program conducted in hybrid mode with live lectures, hands-on and interactive sessions. The hands-on sessions will provide the in-depth knowledge of RTL to GDS flow using Cadence at 180nm GSDK Library.

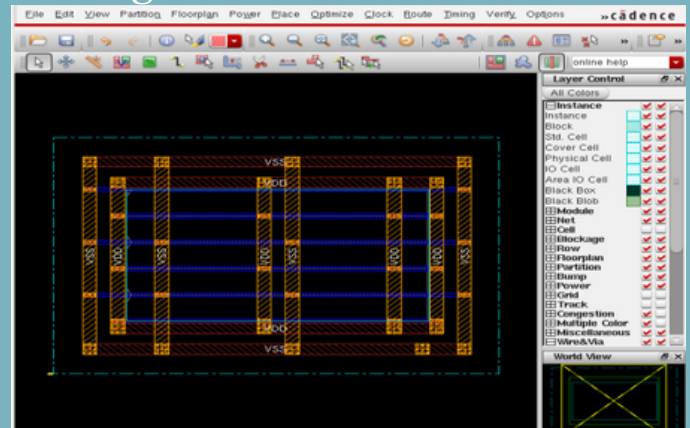
### Highlight of the programme

- Idea about the Verilog HDL, DFT Synthesis
- Import and floorplan your design
- Placement of the standard cells in the design
- Run power planning and power routing
- Incorporation of soft IP in floorplan, placement, routing etc.

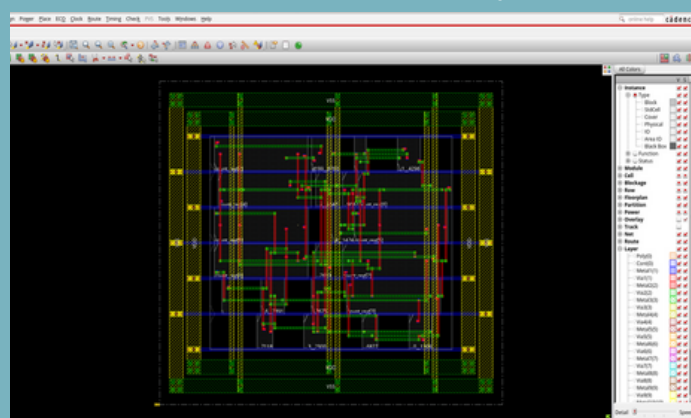
### Floorplan, and Power planning



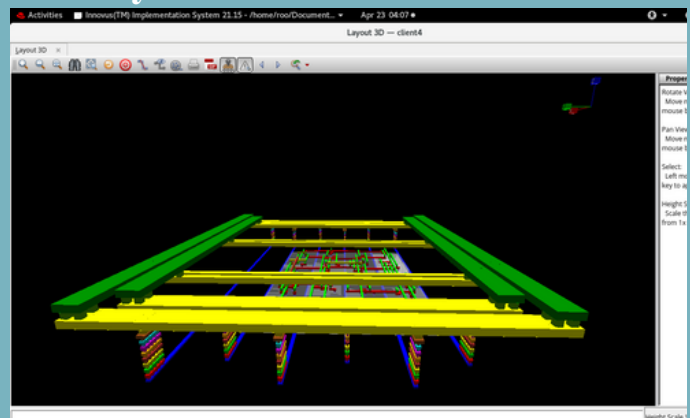
### Routing



### Placement and clock tree synthesis



### 3D Physical view



Registration Link::

<https://forms.gle/jHgexJcHWlqGB2yA6>

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